EXHIBIT 1

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Willamette** Processor Software Developer's Guide

February, 2000

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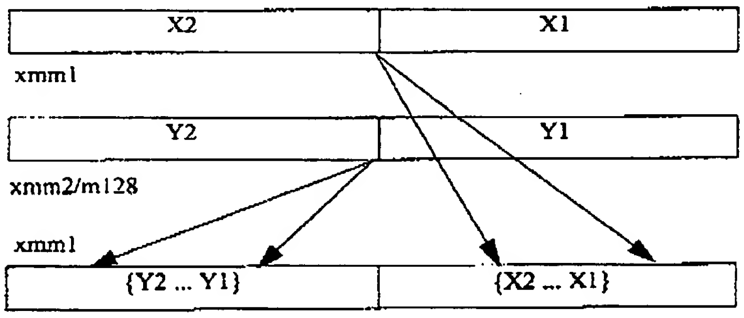
APPENDIX A
STREAMING SIMD EXTENSIONS 2 INSTRUCTION SUMMARY

SHUFPD—Shuffle Double-Precision Floating-Point

Instruction	Description
SHUFPD xmm1, xmm2/m128, imm8	Shuffle packed double-precision floating-point numbers.

Description

Shuffles either of the two packed double-precision floating-point numbers from xmm1 to the low quadword of xmm1; shuffles either of the two packed double-precision floating-point numbers from xmm2/m128 to the high quadword of xmm1. Bit 0 of the immediate field selects which of the two input double-precision floating-point numbers will be put in the low quadword of the result; bit 1 selects which of the two input double-precision floating-point numbers will be put in the high quadword of the result.



Operation

```
fp_select  = (imm8 >> 0) & 0x1;
xmm1[63-0] =        (fp_select == 0) ? xmm1[63-0]  :
                    (fp_select == 1) ? xmm1[127-64];
fp_select  = (imm8 >> 1) & 0x1;
xmm1[127-64] =      (fp_select == 0) ? xmm2/m128[63-0]  :
                    (fp_select == 1) ? xmm2/m128[127-64];
```

Protected Mode Exceptions

#GP(0)	For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0)	For an illegal address in the SS segment.
#PF(fault-code)	For a page fault.

#NM	If TS bit in CR0 is set.
#XM	For an unmasked Streaming SIMD Extensions 2 instructions numeric exception (CR4.OSXMMEXCPT =1).
#UD	For an unmasked Streaming SIMD Extensions 2 instructions numeric exception (CR4.OSXMMEXCPT =0).
	If CR0.EM = 1.
	If CR4.OSFXSR(bit 9) = 0.
	If CPUID.WNI(EDX bit 26) = 0.

Real-Address Mode Exceptions

#GP(0)	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
Interrupt 13	If any part of the operand lies outside the effective address space from 0 to 0FFFFH.
#NM	If TS bit in CR0 is set.
#XM	For an unmasked Streaming SIMD Extensions 2 instructions numeric exception (CR4.OSXMMEXCPT =1).
#UD	For an unmasked Streaming SIMD Extensions 2 instructions numeric exception (CR4.OSXMMEXCPT =0).
	If CR0.EM = 1.
	If CR4.OSFXSR (bit 9) = 0.
	If CPUID.WN(EDX bit 26) = 0.

Virtual-8086 Mode Exceptions

Same exceptions as in Real Address Mode

#PF(fault-code)	For a page fault.

Numeric Exceptions

None.

PSHUFD—Packed Shuffle Doubleword

Instruction	Description
PSHUFD xmm1, xmm2/m128, imm8	Shuffle the doublewords in xmm2/mem128 based on the encoding in imm8 and store result in xmm1.

Description

Shuffles the four doublewords in xmm2/mem128 in the order selected by imm8 and stores the result in xmm1. Bits 1 and 0 of imm8 encode the source for destination doubleword 0 (xmm1[31-0]), bits 3 and 2 encode for doubleword 1, bits 5 and 4 encode for doubleword 2, and bits 7 and 6 encode for doubleword 3 (xmm1[127-96]). Similarly, the two bit encoding represents which source doubleword is to be used, e.g., an binary encoding of 10 indicates that source doubleword 2 (xmm2/mem128[95-64]) will be used.

Operation

```
xmm1[31-0]   = (xmm2/m128 >> (imm8[1-0] * 32) )[31-0]
xmm1[63-32]  = (xmm2/m128 >> (imm8[3-2] * 32) )[31-0]
xmm1[95-64]  = (xmm2/m128 >> (imm8[5-4] * 32) )[31-0]
xmm1[127-96] = (xmm2/m128 >> (imm8[7-6] * 32) )[31-0]
```

Protected Mode Exceptions

#GP(0)	For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0)	For an illegal address in the SS segment.
#PF(fault-code)	For a page fault.
#NM	If TS bit in CR0 is set.
#UD	If CR0.EM = 1.
	If CR4.OSFXSR(bit 9) = 0.
	If CPUID.WNI(EDX bit 26) = 0.

Real-Address Mode Exceptions

#GP(0)	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
Interrupt 13	If any part of the operand lies outside the effective address space from 0 to 0FFFFH.
#NM	If TS bit in CR0 is set.

#UD	If CR0.EM = 1.
	If CR4.OSFXSR (bit 9) = 0.
	If CPUID.WN(EDX bit 26) = 0.

Virtual-8086 Mode Exceptions

Same exceptions as in Real Address Mode

#PF(fault-code)	For a page fault.

Numeric Exceptions

None.

PSHUFHW—Packed Shuffle High Words

Instruction	Description
PSHUFHW xmm1, xmm2/m128, imm8	Shuffle the high words in xmm2/mem128 based on the encoding in imm8 and store the result in xmm1.

Description

Shuffles the four high words in xmm2/mem128 in the order selected by imm8 and stores the result in the high quadword of xmm1. Bits 1 and 0 of imm8 encode the source for destination word 4 (xmm1[79-64]), bits 3 and 2 encode for word 5, bits 5 and 4 encode for word 6, and bits 7 and 6 encode for word 7 (xmm1[127-112]). Similarly, the two bit encoding represents which source word is to be used, e.g., a binary encoding of 10 indicates that source word 6 (XMM2[111-96] or Mem[111-96]) will be used. The low quadword of the destination register is written with the low 64 bits of the source register.

Operation

```
if (source == m128) {
    xmm1[79-64]   = (m128 >> (imm8[1-0] * 16) )[79-64]
    xmm1[95-80]   = (m128 >> (imm8[3-2] * 16) )[79-64]
    xmm1[111-96]  = (m128 >> (imm8[5-4] * 16) )[79-64]
    xmm1[127-112] = (m128 >> (imm8[7-6] * 16) )[79-64]

    xmm1[63-0] = m128[63-0];
} else {
    xmm1[79-64]   = (xmm2 >> (imm8[1-0] * 16) )[79-64]
    xmm1[95-80]   = (xmm2 >> (imm8[3-2] * 16) )[79-64]
    xmm1[111-96]  = (xmm2 >> (imm8[5-4] * 16) )[79-64]
    xmm1[127-112] = (xmm2 >> (imm8[7-6] * 16) )[79-64]

    xmm1[63-0] = xmm2[63-0];
}
```

Protected Mode Exceptions

#GP(0)	For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0)	For an illegal address in the SS segment.
#PF(fault-code)	For a page fault.
#NM	If TS bit in CR0 is set.
#UD	If CR0.EM = 1.

	If CR4.OSFXSR(bit 9) = 0.
	If CPUID.WNI(EDX bit 26) = 0.

Real-Address Mode Exceptions

#GP(0)	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
Interrupt 13	If any part of the operand lies outside the effective address space from 0 to 0FFFFH.
#NM	If TS bit in CR0 is set.
#UD	If CR0.EM = 1.
	If CR4.OSFXSR (bit 9) = 0.
	If CPUID.WN(EDX bit 26) = 0.

Virtual-8086 Mode Exceptions

Same exceptions as in Real Address Mode

#PF(fault-code)	For a page fault.

Numeric Exceptions

None.

PSHUFLW—Packed Shuffle Low Word

Instruction	Description
PSHUFLW xmm1, xmm2/m128, imm8	Shuffle the low words in xmm2/mem128 based on the encoding in imm8 and store in xmm1.

Description

Shuffles the four low words in xmm2/mem128 in the order selected by imm8 and stores the result in the low quadword of xmm1.Bits 1 and 0 of imm8 encode the source for destination word 0 (xmm1[15-0]), bits 3 and 2 encode for word 1, bits 5 and 4 encode for word 2, and bits 7 and 6 encode for word 3 (xmm1[63-48]). Similarly, the two bit encoding represents which source word is to be used, e.g., an binary encoding of 10 indicates that source word 2 (xmm2/mem128[47-32]) will be used. The high quadword of the destination register is written with the high 64 bits of the source register.

Operation

```
if (source == m128) {
    xmm1[15-0]  = (m128 >> (imm8[1-0] * 16) )[15-0]
    xmm1[31-16] = (m128 >> (imm8[3-2] * 16) )[15-0]
    xmm1[47-32] = (m128 >> (imm8[5-4] * 16) )[15-0]
    xmm1[63-48] = (m128 >> (imm8[7-6] * 16) )[15-0]

    xmm1[127-64] = m128[127-64];
} else {
    xmm1[15-0]  = (xmm2 >> (imm8[1-0] * 16) )[15-0]
    xmm1[31-16] = (xmm2 >> (imm8[3-2] * 16) )[15-0]
    xmm1[47-32] = (xmm2 >> (imm8[5-4] * 16) )[15-0]
    xmm1[63-48] = (xmm2 >> (imm8[7-6] * 16) )[15-0]

    xmm1[127-64] = xmm2[127-64];
}
```

Protected Mode Exceptions

#GP(0)	For an illegal memory operand effective address in the CS, DS, ES, FS or GS segments.
	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
#SS(0)	For an illegal address in the SS segment.
#PF(fault-code)	For a page fault.
#NM	If TS bit in CR0 is set.
#UD	If CR0.EM = 1.

	If CR4.OSFXSR(bit 9) = 0.
	If CPUID.WNI(EDX bit 26) = 0.

Real-Address Mode Exceptions

#GP(0)	If memory operand is not aligned on a 16-byte boundary, regardless of segment.
Interrupt 13	If any part of the operand lies outside the effective address space from 0 to 0FFFFH.
#NM	If TS bit in CR0 is set.
#UD	If CR0.EM = 1.
	If CR4.OSFXSR (bit 9) = 0.
	If CPUID.WN(EDX bit 26) = 0.

Virtual-8086 Mode Exceptions

Same exceptions as in Real Address Mode

#PF(fault-code)	For a page fault.

Numeric Exceptions

None.